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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An integrated circuit comprising:

a memory array having a first side;

a self-timing signal-producing circuit located at the first side;

a self-timing signal-reading circuit located at the first side; and

a routing path connecting the self-timing signal-producing circuit to the self-timing signal-reading circuit, wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array.

2. (Original) The integrated circuit of claim 1, wherein the self-timing signal-producing circuit is a dummy row decoder circuit.

3. (Original) The integrated circuit of claim 1, wherein the self-timing signal-producing circuit is a dummy memory cell.

4. (Original) The integrated circuit of claim 3, wherein the self-timing signal-reading circuit is a dummy sense amplifier.

5. (Original) The integrated circuit of claim 1, wherein the memory array is a segment of a larger segmented memory array.

6. (Original) The integrated circuit of claim 5, wherein the larger segmented memory array includes a second segment, and the second segment made up of memory cells that are disabled through metal programming.

7. (Original) The integrated circuit of claim 6, further comprising:

a second routing path, wherein the second routing path is routed over the second segment.

8. (Original) The integrated circuit of claim 1, further comprising:

a programmable logic circuit coupled to the memory array, wherein the memory array outputs data as a single column of bit lines and the programmable logic circuit is programmed to derive a word of a desired word size from the single column of bit lines.

9. (Original) The integrated circuit of claim 8, wherein the programmable logic circuit is programmed to behave as a multiplexer and the word of the desired word size is derived from the single column of bit lines by the multiplexer's selecting a subset of the bit lines from the single column of bit lines.

10. (Original) The integrated circuit of claim 1, wherein the routing path extends into the memory array to a point that is at some intermediate location between the first side and a second side of the memory array, such that a wire delay associated with the routing path approximates a wire delay that would be experienced on a hypothetical routing path extending from the first side to the second side.

11-20. (Canceled)